IP175C

EEPROM Description

Application Note

Rev. 020

Contents

1. IP175C EEPROM description

1.1. Register 0x00(00): EEPROM enable register (Value=8'hAA)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'hAA	30.0[7:0]

1.2. Register 0x01(01): EEPROM enable register (Value=8'h55)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'h55	30.0[15:8]

1.3. Register 0x02(02): switch control register (Value=8'h03)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5	--	Reserved		0	
4	MII2_EN	MII2_EN 1: enable, 0: disable (default)	R/W	0	31.5[2]
3	--	Reserved		0	
2	MII2_MAC_MOD	MII2_MAC_MOD 1: MII2 works in MAC mode 0: MII2 works in PHY mode (default)	R/W	0	31.5[0]
1:0	LED_SEL [1:0]	LED_SEL [1:0] LED mode selection. LED_SEL[1:0]=2'b00: LED mode 0, LED_SEL[1:0]=2'b01: LED mode 1, LED_SEL[1:0]=2'b10: LED mode 2, LED_SEL[1:0]=2'b11: LED mode 3 (default) It is for debug only. User should not update the setting of LED_SEL pins by writing this registers.	R/W	2'b11	29.18[15:14]

1.4. Register 0x03(03): switch control register (Value=8'h0F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5	MII2_RMII_EN	MII2_RMII_EN 1: MII2 RMII interface enabled 0: MII2 RMII interface disabled (default)	R/W	0	31.5[9]
4	MII1_RMII_EN	MII1_RMII_EN 1: MII1 RMII interface enabled 0: MII1 RMII interface disabled (default)	R/W	0	31.5[8]
3	MII1OR2_MAC_REPEATER	MII1OR2_MAC_REPEATER 1: external PHY 's TXEN does not loop back to CRS (default) 0: external PHY 's TXEN loop back to CRS	R/W	1	31.5[7]
2	MII0_MAC_REPEATER	MII0_MAC_REPEATER 1: external PHY 's TXEN does not loop back to CRS (default) 0: external PHY 's TXEN loop back to CRS	R/W	1	31.5[6]
1	MII2_PHY_COL_DELAY	MII2_PHY_COL_DELAY 0: no delay 1: collision delay 24 clocks (default) It is valid only if MII2 is enabled and it works at PHY mode.	R/W	1	31.5[5]
0	MII0_PHY_COL_DELAY	MII0_PHY_COL_DELAY 0: no delay 1: collision delay 24 clocks (default) It is valid only if MII0 is enabled and it works at PHY mode.	R/W	1	31.5[4]

1.5. Register 0x04(04): switch control register (Value=8'h98)

Bit	Signal name	Description	R/W	Default	MII_reg
7	X_EN	IEEE 802.3x flow control enable This signal is used as pause_en for digital parts. 1: enable (default) 0: disable	R/W	1	29.18[13]
6:5	--	Reserved		2'b00	
4	BK_EN	Backpressure enable 1: enable (default) 0: disable	R/W	1	29.18[12]
3	MAC_X_EN	MAC_X_EN, MII0 flow control enable 1: enable (default) 0: disable	R/W	1	29.18[10]
2	BF_STM_EN	Broadcast storm enable 1: enable Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is 32 unit. One unit is 128 bytes. 0: disable (default)	R/W	0	29.18[11]
1:0	--	Reserved		2'b00	

1.6. Register 0x05(05): switch control register (Value=8'h01)

Bit	Signal name	Description (Switch control register 1)	R/W	Default	MII_reg
7:4	--	Reserved		4'h0	
3	bp_kind	bp_kind	R/W	0	30.18[8]
2:1	--	Reserved		2'b00	
0	MBSTM DISABLE	MBSTM DISABLE Multicast broadcast storm protection disable 1: "Broadcast storm protection"does not include multicast packets. IP175C drops the packets with DA = FFFFFFFF only when the broadcast threshold is reached (default). 0: "Broadcast storm protection"includes multicast packets. IP175C drops the packets with DA = FFFFFFFF, or multi-cast address when the broadcast threshold is reached. "Broadcast storm protection" does not drop packets due to notlearned address.	R/W	1	30.27[8]

1.7. Register 0x06(06): switch control register (Value=8'h16)

ROM	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6	--	Reserved		0	
5	HASH_MODE	HASH_MODE It is latched as Hashing algorithm selection for 1st layer and 2nd layer at the end of reset. 0: direct and CRC (default) 1: direct and CRC	R/W	0	29.18[4]
4	AGING	AGING Aging time of address table selection An address tag in hashing table will be dropped if this function is turned on and its aging timer expires. Aging =bit[4] 0: no aging 1: aging time 280sec (default)	R/W	1	29.18[3]

3	--	Reserved		0	
2	twopart	twopart	R/W	1	30.18[9]
1	modbck	modbck	R/W	1	30.18[10]
0	--	Reserved		0	

1.8. Register 0x07(07): switch control register (Value=8'h10)

Bit	Signal name	Description (Switch control register 1)	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4	MII1_PHY_MOD	MII1_PHY_MOD 1:MII1 is connected to PHY4 (default) 0:MII1 is connected to MAC4	R/W	1	31.5[12]
3:1	--	Reserved		3'h0	
0	P4EXT	P4EXT 1: enable 0: disable (default)	R/W	0	31.5[15]

1.9. Register 0x08(08): (Value=8'h00)

Bit	Signal name	Description (Switch control register 1)	R/W	Default	MII_reg
7:0	--	Reserved		8'h00	

1.10. Register 0x09(09): (Value=8'h03)

Bit	Signal name	Description (Switch control register 1)	R/W	Default	MII_reg
7:2	--	Reserved		6'h00	
1	MDIX_FORCE	MDIX_FORCE 1:enable (default) 0:disable	R/W	1	31.6[1]
0	EN_AUTOMDIX	EN_AUTOMDIX 1: enable auto mdi/mdix function (default), It is valid only if MII 31.6.1 mdix_force is equal to 1 or Nway is enabled. 0: disable auto mdi/mdix function	R/W	1	31.6[0]

1.11. Register 0x0A(10): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5	DIGITAL_SPEED_UP	DIGITAL_SPEED_UP	R/W	0	30.17[11]
4	DIGITAL_LPBK	DIGITAL_LPBK	R/W	0	30.17[10]
3:2	--	Reserved		2'b00	
1	BYSCR_MODE	BYSCR_MODE	R/W	0	30.17[9]
0	--	Reserved		0	

1.12. Register 0x0B(11): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:4	Drive	Drive Pad driving capability selection 00: 4mA (default) 01: 8mA 10: 12mA 11: 16mA	R/W	2'b00	30.17[14:13]
3	F_LINK_100	F_LINK_100	R/W	0	30.17[8]

2	F_LINK_10	F_LINK_10	R/W	0	30.17[7]
1	SPEED_UP_10	SPEED_UP_10	R/W	0	30.17[6]
0	--	Reserved		0	

1.13. Register 0x0C(12): Testing & allpass (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6	allpass	allpass	R/W	0	30.18[11]
5:0	TMOD_SEL	TMOD_SEL	R/W	6'h00	30.17[5:0]

1.14. Register 0x0D(13): (Value=8'h9F)

Bit	Signal name	Description	R/W	Default	MII_reg
7	Port5 VLAN look up table	Port5 VLAN look up table Port5 and port5 are in the same VLAN. This bit is "don't care". It is fixed "1".	R/W	1	30.18[7]
6	Port5 Class of service enable	Port5 Class of service enable 1: enable, 0: disabled (default) Packets with high priority tag from Port5 are handled as high priority packets.	R/W	0	30.18[6]
5	Port5 set to be high priority port	Port5 set to be high priority port 1: enable, 0: disabled (default) Packets received from Port5 are handled as high priority packets.	R/W	0	30.18[5]
4:0	Port5 VLAN look up table	Port5 VLAN look up table The register defines the ports in the same VLAN as port5. The bit 0~5 are corresponding to port 0~5. 1: a port is in the same VLAN as Port5 0: a port is not in the same VLAN as MI port Bit0=1, port 0 and Port5 are in the same VLAN; Bit1=1, port 1 and Port5 are in the same VLAN; Bit2=1, port 2 and Port5 are in the same VLAN; Bit3=1, port 3 and Port5 are in the same VLAN; Bit4=1, port 4 and Port5 are in the same VLAN; Bit5=1, don't care;	R/W	5'h1f	30.18[4:0]

1.15. Register 0x0E(14): VLAN register 0 (Value=8'h9F)

bit	Signal name	Description	R/W	Default	MII_reg
7	vlan_0[5]	Port0 VLAN look up table Port5 and port0 are in the same VLAN	R/W	1	29.19[15]
6	p_cos[0]	Port0 Class of service enable 1: enable 0: disabled (default) Packets with high priority tag from port0 are handled as high priority packets.	R/W	0	29.19[14]
5	p_high[0]	Port0 set to be high priority port 1: enable 0: disabled (default) Packets received from port0 are handled as high priority packets.	R/W	0	29.19[13]

4:0	vlan_0[4:0]	Port0 VLAN look up table The register defines the ports in the same VLAN with port0. The bit 0~4 are corresponding to port 0~4. 1: a port is in the same VLAN as port0 0: a port is not in the same VLAN as port0 Bit8, don't care; Bit9=1, port 1 and port0 are in the same VLAN; Bit10=1, port 2 and port0 are in the same VLAN; Bit11=1, port 3 and port0 are in the same VLAN; Bit12=1, port 4 and port0 are in the same VLAN	R/W	5'h1f	29.19[12:8]

1.16. Register 0x0F(15): VLAN register 1 (Value=8'h9F)

Bit	Signal name	Description	R/W	Default	MII_reg
7	vlan_1[5]	Port1 VLAN look up table Port5 and port1 are in the same VLAN	R/W	1	29.19[7]
6	p_cos[1]	Port1 Class of service enable 1: enable 0: disabled (default) Packets with high priority tag from port1 are handled as high priority packets.	R/W	0	29.19[6]
5	p_high[1]	Port1 set to be high priority port 1: enable 0: disabled (default) Packets received from port1 are handled as high priority packets.	R/W	0	29.19[5]
4:0	vlan_1[4:0]	Port1 VLAN look up table The register defines the ports in the same VLAN with port1. The bit 0~4 are corresponding to port 0~4. 1: a port is in the same VLAN as port1 0: a port is not in the same VLAN as port1 Bit8=1, port 0 and port1 are in the same VLAN; Bit9=, don't care; Bit10=1, port 2 and port1 are in the same VLAN; Bit11=1, port 3 and port1 are in the same VLAN; Bit12=1, port 4 and port1 are in the same VLAN	R/W	5'h1f	29.19[4:0]

1.17. Register 0x10(16): VLAN register 2 (Value=8'h9F)

Bit	Signal name	Description	R/W	Default	MII_reg
7	vlan_2[5]	Port2 VLAN look up table Port5 and port2 are in the same VLAN	R/W	1	29.20[15]
6	p_cos[2]	Port2 Class of service enable 1: enable 0: disabled (default) Packets with high priority tag from port2 are handled as high priority packets.	R/W	0	29.20[14]
5	p_high[2]	Port2 set to be high priority port 1: enable 0: disabled (default) Packets received from port2 are handled as high priority packets.	R/W	0	29.20[13]

4:0	vlan_2[4:0]	Port2 VLAN look up table The register defines the ports in the same VLAN with port2. The bit 0~4 are corresponding to port 0~4. 1: a port is in the same VLAN as port2 0: a port is not in the same VLAN as port2 Bit8=1, port 0 and port2 are in the same VLAN; Bit9=1, port 1 and port2 are in the same VLAN; Bit10, don't care; Bit11=1, port 3 and port2 are in the same VLAN; Bit12=1, port 4 and port2 are in the same VLAN	R/W	5'h1f	29.20[12:8]

1.18. Register 0x11(17): VLAN register 3 (Value=8'h9F)

Bit	Signal name	Description (VLAN register 3)	R/W	Default	MII_reg
7	Vlan_3[5]	Port3 VLAN look up table Port5 and port3 are in the same VLAN	R/W	1	29.20[7]
6	P_cos[3]	Port3 Class of service enable 1: enable 0: disabled (default) Packets with high priority tag from port3 are handled as high priority packets.	R/W	0	29.20[6]
5	P_high[3]	Port3 set to be high priority port 1: enable 0: disabled (default) Packets received from port3 are handled as high priority packets.	R/W	0	29.20[5]
4:0	Vlan_3[4:0]	Port3 VLAN look up table The register defines the ports in the same VLAN with port3. The bit 0~4 are corresponding to port 0~4. 1: a port is in the same VLAN as port3 0: a port is not in the same VLAN as port3 Bit8=1, port 0 and port3 are in the same VLAN; Bit9=1, port 1 and port3 are in the same VLAN; Bit10=1, port 2 and port3 are in the same VLAN; Bit11, don't care; Bit12=1, port 4 and port3 are in the same VLAN	R/W	5'h1f	29.20[4:0]

1.19. Register 0x12(18): VLAN register 4 (Value=8'h9F)

Bit	Signal name	Description	R/W	Default	MII_reg
7	vlan_4[5]	Port4 VLAN look up table Port5 and port4 are in the same VLAN	R/W	1	29.21[15]
6	p_cos[4]	Port4 Class of service enable 1: enable 0: disabled (default) Packets with high priority tag from port4 are handled as high priority packets.	R/W	0	29.21[14]
5	p_high[4]	Port4 set to be high priority port 1: enable 0: disabled (default) Packets received from port4 are handled as high priority packets.	R/W	0	29.21[13]

4:0	vlan_4[4:0]	Port4 VLAN look up table The register defines the ports in the same VLAN with port4. The bit 0~4 are corresponding to port 0~4. 1: a port is in the same VLAN as port4 0: a port is not in the same VLAN as port4 Bit8=1, port 0 and port4 are in the same VLAN Bit9=1, port 1 and port4 are in the same VLAN; Bit10=1, port 2 and port4 are in the same VLAN; Bit11=1, port 3 and port4 are in the same VLAN; Bit12, don't care;	R/W	5'h1f	29.21[12:8]

1.20. Register 0x13(19): FORCE MODE (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4	P4_FORCE	P4_FORCE Port4 force mode enable 1: enable force mode 0: disable force mode, port4 NWAY with all capability	R/W	0	29.22[15]
3	P3_FORCE	P3_FORCE Port3 force mode enable 1: enable force mode 0: disable force mode, port3 NWAY with all capability	R/W	0	29.22[14]
2	P2_FORCE	P2_FORCE Port2 force mode enable 1: enable force mode 0: disable force mode, port2 NWAY with all capability	R/W	0	29.22[13]
1	P1_FORCE	P1_FORCE Port1 force mode enable 1: enable force mode 0: disable force mode, port1 NWAY with all capability	R/W	0	29.22[12]
0	P0_FORCE	P0_FORCE Port0 force mode enable 1: enable force mode 0: disable force mode, port0 NWAY with all capability	R/W	0	29.22[11]

1.21. Register 0x14(20): FORCE SPEED (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4	P4_FORCE 100	P4_FORCE100 Force port4 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p4_force (21[15]) is set to 1'b1.	R/W	0	29.22[10]
3	P3_FORCE 100	P3_FORCE100 Force port3 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p3_force (21[14]) is set to 1'b1.	R/W	0	29.22[9]
2	P2_FORCE 100	P2_FORCE100 Force port2 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p2_force (21[13]) is set to 1'b1.	R/W	0	29.22[8]

1	P1_FORCE 100	P1_FORCE100 Force port1 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p1_force (21[12]) is set to 1'b1.	R/W	0	29.22[7]
0	P0_FORCE 100	P0_FORCE100 Force port0 to be 100M 1: force to be 100M 0: force to be 10M It is valid only if p0_force (21[11]) is set to 1'b1.	R/W	0	29.22[6]

1.22. Register 0x15(21): FORCE FULL DUPLEX (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4	P4_FORCE_FULL	P4_FORCE_FULL Force port4 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.15) is set to 1'b1.	R/W	0	29.22[5]
3	P3_FORCE_FULL	P3_FORCE_FULL Force port3 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.14) is set to 1'b1.	R/W	0	29.22[4]
2	P2_FORCE_FULL	P2_FORCE_FULL Force port2 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.13) is set to 1'b1.	R/W	0	29.22[3]
1	P1_FORCE_FULL	P1_FORCE_FULL Force port1 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.12) is set to 1'b1.	R/W	0	29.22[2]
0	P0_FORCE_FULL	P0_FORCE_FULL Force port0 to be full duplex 1: force full duplex 0: force half duplex It is valid only if p4_force (15.11) is set to 1'b1.	R/W	0	29.22[1]

1.23. Register 0x16(22): add vlan tag (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5	ADD_TAG	ADD_TAG. Add VLAN tag 1: Port5 adds a VLAN tag to each outgoing packet 0: Port5 doesn't adds a VLAN tag	R/W	0	29.23[1]
4:0	ADD_TAG	ADD_TAG. Add VLAN tag Port4~0 adds a VLAN tag defined in vlan_tag_4~0 to each outgoing packet	R/W	5'h00	29.23[15:11]

1.24. Register 0x17(23): remove vlan tag (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5	REMOVE_TAG	REMOVE_TAG. Remove VLAN tag 1: Port5 removes the VLAN tag of each outgoing packet. 0: Port5 doesn't removes the VLAN tag of each outgoing packet.		0	29.23[0]

4:0	REMOVE_TAG	REMOVE_TAG. Remove VLAN tag	R/W	5'h00	29.23[10:6]

1.25. Register 0x18(24): port0 vlan control info (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_0	VLAN_TAG_0. Port0 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 0.	R/W	8'h01	29.24[7:0]

1.26. Register 0x19(25): port0 vlan control info (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_0	VLAN_TAG_0. Port0 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 0.	R/W	8'h00	29.24[15:8]

1.27. Register 0x1A(26): port1 vlan control info (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_1	VLAN_TAG_1. Port1 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 1.	R/W	8'h01	29.25[7:0]

1.28. Register 0x1B(27): port1 vlan control info (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_1	VLAN_TAG_1. Port1 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 1.	R/W	8'h00	29.25[15:8]

1.29. Register 0x1C(28): port2 vlan control info (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_2	VLAN_TAG_2. Port2 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 2.	R/W	8'h01	29.26[7:0]

1.30. Register 0x1D(29): port2 vlan control info (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_2	VLAN_TAG_2. Port2 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 2.	R/W	8'h00	29.26[15:8]

1.31. Register 0x1E(30): port3 vlan control info (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_3	VLAN_TAG_3. Port3 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 3.	R/W	8'h01	29.27[7:0]

1.32. Register 0x1F(31): port3 vlan control info (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_3	VLAN_TAG_3. Port3 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 3.	R/W	8'h00	29.27[15:8]

1.33. Register 0x20(32): port4 vlan control info (Value=8'h02)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_4	VLAN_TAG_4. Port4 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 4.	R/W	8'h02	29.28[7:0]

1.34. Register 0x21(33): port4 vlan control info (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_4	VLAN_TAG_4. Port4 default VLAN tag value This register defines the VLAN tag of an un-tagged packet from port 4.	R/W	8'h00	29.28[15:8]

1.35. Register 0x22(34): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'h00	

1.36. Register 0x23(35): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	REG29SW[7:0]	REG29SW[7:0]- reserved	R/W	8'h00	29.29[7:0]

1.37. Register 0x24(36): (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	REG29SW[15:8]	REG29SW[15:8]- reserved	R/W	8'h01	29.29[15:8]

1.38. Register 0x25(37): port5 vlan control info (Value=8'h02)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_5[7:0]	VLAN_TAG_5. Port5 default VALN tag value. This register defines the VLAN tag of an un-tagged packet from port 5.	R/W	8'h02	29.30[15:8]

1.39. Register 0x26(38): port5 vlan control info (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	VLAN_TAG_5[15:8]	VLAN_TAG_5. Port5 default VALN tag value. This register defines the VLAN tag of an un-tagged packet from port 5.	R/W	8'h00	29.30[15:8]

1.40. Register 0x27(39): tag_vlan_mask0 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_0[5:0].	TAG_VLAN_MASK_0[5:0]. Tag VLAN 0 output port mask The mask is valid only if MII register 9.7 TAG_VLAN_EN is logic high and VID index is 4'b0000. When IP175C receives a packet, it examines the VID index to choose a tag VLAN mask and forwards the packets according MAC address table and the mask.	R/W	6'h3f	30.1[5:0]

1.41. Register 0x28(40): tag_vlan_mask1 (Value=8'h2F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_1[5:0].	TAG_VLAN_MASK_1[5:0]. Tag VLAN 1 output port mask	R/W	6'h2f	30.1[13:8]

1.42. Register 0x29(41): tag_vlan_mask2 (Value=8'h30)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_2[5:0].	TAG_VLAN_MASK_2[5:0]. Tag VLAN 2 output port mask	R/W	6'h30	30.2[5:0]

1.43. Register 0x2A(42): tag_vlan_mask3 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_3[5:0].	TAG_VLAN_MASK_3[5:0]. Tag VLAN 3 output port mask	R/W	6'h3f	30.2[13:8]

1.44. Register 0x2B(43): tag_vlan_mask4 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_4[5:0].	TAG_VLAN_MASK_4[5:0]. Tag VLAN 4 output port mask	R/W	6'h3f	30.3[5:0]

1.45. Register 0x2C(44): tag_vlan_mask5 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_5[5:0].	TAG_VLAN_MASK_5[5:0]. Tag VLAN 5 output port mask	R/W	6'h3f	30.3[13:8]

1.46. Register 0x2D(45): tag_vlan_mask6 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_6[5:0].	TAG_VLAN_MASK_6[5:0]. Tag VLAN 6 output port mask	R/W	6'h3f	30.4[5:0]

1.47. Register 0x2E(46): tag_vlan_mask7 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_7[5:0].	TAG_VLAN_MASK_7[5:0]. Tag VLAN 7 output port mask	R/W	6'h3f	30.4[13:8]

1.48. Register 0x2F(47): tag_vlan_mask8 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_8[5:0].	TAG_VLAN_MASK_8[5:0]. Tag VLAN 8 output port mask	R/W	6'h3f	30.5[5:0]

1.49. Register 0x30(48): tag_vlan_mask9 (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_9[5:0].	TAG_VLAN_MASK_9[5:0]. Tag VLAN 9 output port mask	R/W	6'h3f	30.5[13:8]

1.50. Register 0x31(49): tag_vlan_maskA (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_A[5:0].	TAG_VLAN_MASK_A[5:0]. Tag VLAN A output port mask	R/W	6'h3f	30.6[5:0]

1.51. Register 0x32(50): tag_vlan_maskB (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_B[5:0].	TAG_VLAN_MASK_B[5:0]. Tag VLAN B output port mask	R/W	6'h3f	30.6[13:8]

1.52. Register 0x33(51): tag_vlan_maskC (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_C[5:0].	TAG_VLAN_MASK_C[5:0]. Tag VLAN C output port mask	R/W	6'h3f	30.7[5:0]

1.53. Register 0x34(52): tag_vlan_maskD (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_D[5:0].	TAG_VLAN_MASK_D[5:0]. Tag VLAN D output port mask	R/W	6'h3f	30.7[13:8]

1.54. Register 0x35(53): tag_vlan_maskE (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_E[5:0].	TAG_VLAN_MASK_E[5:0]. Tag VLAN E output port mask	R/W	6'h3f	30.8[5:0]

1.55. Register 0x36(54): tag_vlan_maskF (Value=8'h3F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	TAG_VLAN_MASK_F[5:0].	TAG_VLAN_MASK_F[5:0]. Tag VLAN F output port mask	R/W	6'h3f	30.8[13:8]

1.56. Register 0x37(55): smart mac register (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7	TAG_VLAN_EN	TAG_VLAN_EN. Enable tag VLAN function 1: enable tag VLAN function 0: disable tag VLAN function	R/W	0	30.9[7]

6:4	VID_SEL	VID_SEL. VID index selection Select 4 bits out of 12 bits VID as index of tag VLAN groups. The 12 bits of VID can't be all zeros; otherwise, it will be handled as an un-tagged frame. 000: VID[3:0], 001: VID[4:1], 010: VID[5:2], 011: VID[6:3], 100: VID[7:4], 101: VID[8:5], 110: VID[9:6], 111: VID[10:7] An example of vid_sel = 3'b000,	R/W	3'b000	30.9[6:4]
3	ROUTER_EN	ROUTER_EN. Enable router function at MII port 1: MAC clone enabled. 0: MAC clone disabled.	R/W	0	30.9[3]
2:0	LAN_GROUPS[2:0]	LAN_GROUPS[2:0]. Number of VLAN groups of LAN ports in a router application It defines the VLANs used by LAN ports. Each VLAN should contain MII port. It is valid only if router_en is enabled. 000: unsupported value 001: 1 VLAN group, (VLAN 1) 010: 2 VLAN groups, (VLAN 1~VLAN 2) 011: 3 VLAN groups, (VLAN 1~VLAN 3) 100: 4 VLAN groups, (VLAN 1~VLAN 4) 101: 5 VLAN groups, (VLAN 1~VLAN 5) 110: 6 VLAN groups, (VLAN 1~VLAN 6) 111: 7 VLAN groups, (VLAN 1~VLAN 7)	R/W	3'b001	30.9[2:0]

1.57. Register 0x38(56): wan port setting (Value=8'h10)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4:0	WAN_PORTS[4:0]	WAN_PORTS[4:0]. WAN ports for router application It is valid only if router_en is enabled.	R/W	5'h10	30.9[12:8]

1.58. Register 0x39(57): port lock (port security) (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	--	Reserved		2'b00	
5:0	PORT_LOCK_EN[5:0]	PORT_LOCK_EN[5:0]. Lock port MAC address 1: enable 0: disable User has to reset IP175C by writing 16'h175C to MII register 30.0 software reset register after enabling this function.	R/W	6'h00	30.10[5:0]

1.59. Register 0x3A(58): queue threshold (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg

7:6	UNIT_HIGH_THR_SEL[1;0]	UNIT_HIGH_THR_SEL[1;0]. The default value should be adopted for normal operation.	R/W	2'b00	30.11[7:6]
5	BF_STM_EN_QM	BF_STM_EN_QM The default value should be adopted for normal operation.	R/W	0	30.11[5]
4	PREDROP_EN	PREDROP_EN 1: Drop an incoming broadcast packet if any port is congested. 0: forward an incoming broadcast packet to un-congested ports instead of congested ports.	R/W	0	30.11[4]
3:2	PKT_LOW_THR_SEL[1:0]	PKT_LOW_THR_SEL[1:0]. The default value should be adopted for normal operation.	R/W	2'b00	30.11[3:2]
1:0	PKT_HIGH_THR_SEL[1:0]	PKT_HIGH_THR_SEL[1:0]. The default value should be adopted for normal operation.	R/W	2'b00	30.11[1:0]

1.60. Register 0x3B(59): queue threshold (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:6	BF_STM_THR_SEL[1:0]	BF_STM_THR_SEL[1:0]. Broadcast storm threshold selection 00: 159 packets/10ms for 100Mbps port, or 159 packets/100ms for 10Mbps port. 01: 127 packets/10ms for 100Mbps port, or 127 packets/100ms for 10Mbps port. 10: 63 packets/10ms for 100Mbps port, or 63 packets/100ms for 10Mbps port. 11: 31 packets/10msfor 100Mbps port, or 31 packets/100ms for 10Mbps port	R/W	2'b00	30.11[15:14]
5:4	SHARE_FULL_THR_SEL[1;0]	The default value should be adopted for normal operation.	R/W	2'b00	30.11[13:12]
3:2	UNIT_DEFAULT_THR_SEL[1:0]	The default value should be adopted for normal operation.	R/W	2'b00	30.11[11:10]
1:0	UNIT_LOW_THR_SEL[1:0]	UNIT_LOW_THR_SEL[1:0] The default value should be adopted for normal operation.	R/W	2'b00	30.11[9:8]

1.61. Register 0x3C(60): switch control register (Value=8'h82)

Bit	Signal name	Description	R/W	Default	MII_reg
7	LINK_Q_EN	LINK_Q_EN, LINK quality enable 1: enable (default), 0: disable	R/W	1	30.12[7]
6	--	Reserved		0	
5	LONG_PACKET	LONG_PACKET Max forwarded packet length 1: 1552 bytes 0: 1536 bytes (default)	R/W	0	30.12[5]
4	PRIORITY_RATE	PRIORITY_RATE 1: 8 packets 0: 4 packets Output Queue Scheduling: high priority packet rate	R/W	0	30.12[4]

3	MII0_RMII_EN	MII0_RMII_EN 1:MII0 RMII interface enable 0:MII0 RMII interface disable (default)	R/W	0	31.5[10]
2	MII0_MAC_MODE_EN	MII0_MAC_MODE_EN External MII0 port MAC mode 1: MII0 works as a MAC and should be connected to an external PHY. 0: MII0 works as a PHY and should be connected to an external MAC device (default). This bit does not affect MII1 port	R/W	0	31.5[11]
1	--	Reserved		1	
0	HP_DIS_FLOW_EN	HP_DIS_FLOW_EN High priority packet to disable flow control 1: a port will disable its flow control function for 2 sec if it receives a high priority packet. 0: the function is disabled	R/W	0	30.12[0]

1.62. Register 0x3D(61): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'h00	

1.63. Register 0x3E(62): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'h00	

1.64. Register 0x3F(63): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'h00	

1.65. Register 0x40(64): (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	--	Reserved		8'h00	

1.66. Register 0x41(65): spanning tree register (Value=8'h1F)

Bit	Signal name	Description	R/W	Default	MII_reg
7	Stag_en	Stag_en special tagging function enable. If this function is enabled, IP175C inserts source port information in tag header. 1: enable special tagging function 0: disable special tagging function	R/W	0	30.16[7]
6:5	--	Reserved		2'b00	
4	Forward enable	Forward enable 1: enable receiving function of port 4 0: disable receiving function of port 4	R/W	1	30.16[4]
3	Forward enable	Forward enable 1: enable receiving function of port 3 0: disable receiving function of port 3	R/W	1	30.16[3]
2	Forward enable	Forward enable 1: enable receiving function of port 2 0: disable receiving function of port 2	R/W	1	30.16[2]
1	Forward enable	Forward enable 1: enable receiving function of port 1 0: disable receiving function of port 1	R/W	1	30.16[1]

0	Forward enable	Forward enable 1: enable receiving function of port 0 0: disable receiving function of port 0	R/W	1	30.16[0]

1.67. Register 0x42(66): spanning tree register (Value=8'h1F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4	Learning enable	Learning enable 1: enable address learning capability of port 4 0: disable address learning capability of port 4	R/W	1	30.16[12]
3	Learning enable	Learning enable 1: enable address learning capability of port 3 0: disable address learning capability of port 3	R/W	1	30.16[11]
2	Learning enable	Learning enable 1: enable address learning capability of port 2 0: disable address learning capability of port 2	R/W	1	30.16[10]
1	Learning enable	Learning enable 1: enable address learning capability of port 1 0: disable address learning capability of port 1	R/W	1	30.16[9]
0	Learning enable	Learning enable 1: enable address learning capability of port 0 0: disable address learning capability of port 0	R/W	1	30.16[8]

1.68. Register 0x43(67): static mac0 (BPDU packet) (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_0[7:0]	static_mac_0[7:0]	R/W	8'h00	30.20[7:0]

1.69. Register 0x44(68): static mac0 (BPDU packet) (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_0[15:8]	static_mac_0[15:8]	R/W	8'h00	30.20[15:8]

1.70. Register 0x45(69): static mac0 (BPDU packet) (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_0[23:16]	static_mac_0[23:16]	R/W	8'h00	30.21[7:0]

1.71. Register 0x46(70): static mac0 (BPDU packet) (Value=8'hC2)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_0[31:24]	static_mac_0[31:24]	R/W	8'hc2	30.21[15:8]

1.72. Register 0x47(71): static mac0 (BPDU packet) (Value=8'h80)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_0[39:32]	static_mac_0[39:32]	R/W	8'h80	30.22[7:0]

1.73. Register 0x48(72): static mac0 (BPDU packet) (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_0[47:40]	static_mac_0[47:40]	R/W	8'h01	30.22[15:8]

1.74. Register 0x49(73): static mac1 (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_1[7:0]	static_mac_1[7:0]	R/W	8'h00	30.23[7:0]

1.75. Register 0x4A(74): static mac1 (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_1[15:8]	static_mac_1[15:8]	R/W	8'h00	30.23[15:8]

1.76. Register 0x4B(75): static mac1 (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_1[23:16]	static_mac_1[23:16]	R/W	8'h00	30.24[7:0]

1.77. Register 0x4C(76): static mac1 (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_1[31:24]	static_mac_1[31:24]	R/W	8'h00	30.24[15:8]

1.78. Register 0x4D(77): static mac1 (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_1[39:32]	static_mac_1[39:32]	R/W	8'h00	30.25[7:0]

1.79. Register 0x4E(78): static mac1 (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	static_mac_1[47:40]	static_mac_1[47:40]	R/W	8'h00	30.25[15:8]

1.80. Register 0x4F(79): spanning tree control register (Value=8'hA0)

Bit	Signal name	Description	R/W	Default	MII_reg
7	static_overide_0	static_overide_0 1: override the transmission, receiving and Learning setting in MII register 30.16. 0: not override	R/W	1	30.26[7]
6	static_valid_0	static_valid_0 1: the entry is valid 0: the entry is not valid	R/W	0	30.26[6]
5:0	static_port_mask_0	static_port_mask_0 Bit [5]: forward to port 5 (MII0) Bit [4]: forward to port 4 Bit [3]: forward to port 3 Bit [2]: forward to port 2 Bit [1]: forward to port 1 Bit [0]: forward to port 0	R/W	6'h20	30.26[5:0]

1.81. Register 0x50(80): spanning tree control register (Value=8'h20)

Bit	Signal name	Description	R/W	Default	MII_reg
7	static_overide_1	static_overide_1 1: override the transmission, receiving and Learning setting in MII register 30.16. 0: not override	R/W	0	30.26[15]
6	Static_valid_1	static_valid_1 1: the entry is valid 0: the entry is not valid	R/W	0	30.26[14]

5:0	static_port_mask_1	static_port_mask_1 Bit [13]: forward to port 5 (MII0) Bit [12]: forward to port 4 Bit [11]: forward to port 3 Bit [10]: forward to port 2 Bit [9]: forward to port 1 Bit [8]: forward to port 0	R/W	6'h20	30.26[13:8]

1.82. Register 0x51(81): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:1	--	Reserved		7'h00	
0	DIFFSEV_EN	DIFFSEV_EN	R/W	0	30.27[0]

1.83. Register 0x52(82): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[7:0]	DSCP[7:0]	R/W	8'h00	30.28[7:0]

1.84. Register 0x53(83): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[15:8]	DSCP[15:8]	R/W	8'h00	30.28[15:8]

1.85. Register 0x54(84): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[23:16]	DSCP[23:16]	R/W	8'h00	30.29[7:0]

1.86. Register 0x55(85): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[31:24]	DSCP[31:24]	R/W	8'h00	30.29[15:8]

1.87. Register 0x56(86): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[39:32]	DSCP[39:32]	R/W	8'h00	30.30[7:0]

1.88. Register 0x57(87): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[47:40]	DSCP[47:40]	R/W	8'h00	30.30[15:8]

1.89. Register 0x58(88): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[55:48]	DSCP[55:48]	R/W	8'h00	30.31[7:0]

1.90. Register 0x59(89): Diffserv (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:0	DSCP[63:56]	DSCP[63:56]	R/W	8'h00	30.31[15:8]

1.91. Register 0x5A(90): port0 BW control (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	

6:4	BW_CONTROL_P0_TX[2:0]	BW_CONTROL_P0_TX[2:0]	R/W	3'h0	31.0[6:4]
3	--	Reserved		0	
2:0	BW_CONTROL_P0_RX[2:0]	BW_CONTROL_P0_RX[2:0]	R/W	3'h0	31.0[2:0]

1.92. Register 0x5B(91): port1 BW control (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6:4	BW_CONTROL_P1_TX[2:0]	BW_CONTROL_P1_TX[2:0]	R/W	3'h0	31.0[14:12]
3	--	Reserved		0	
2:0	BW_CONTROL_P1_RX[2:0]	BW_CONTROL_P1_RX[2:0]	R/W	3'h0	31.0[10:8]

1.93. Register 0x5C(92): port2 BW control (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6:4	BW_CONTROL_P2_TX[2:0]	BW_CONTROL_P2_TX[2:0]	R/W	3'h0	31.1[6:4]
3	--	Reserved		0	
2:0	BW_CONTROL_P2_RX[2:0]	BW_CONTROL_P2_RX[2:0]	R/W	3'h0	31.1[2:0]

1.94. Register 0x5D(93): port3 BW control (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6:4	BW_CONTROL_P3_TX[2:0]	BW_CONTROL_P3_TX[2:0]	R/W	3'h0	31.1[14:12]
3	--	Reserved		0	
2:0	BW_CONTROL_P3_RX[2:0]	BW_CONTROL_P3_RX[2:0]	R/W	3'h0	31.1[10:8]

1.95. Register 0x5E(94): port4 BW control (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6:4	BW_CONTROL_P4_TX[2:0]	BW_CONTROL_P4_TX[2:0]	R/W	3'h0	31.2[6:4]
3	--	Reserved		0	
2:0	BW_CONTROL_P4_RX[2:0]	BW_CONTROL_P4_RX[2:0]	R/W	3'h0	31.2[2:0]

1.96. Register 0x5F(95): port5 BW control (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7	--	Reserved		0	
6:4	BW_CONTROL_P5_TX[2:0]	BW_CONTROL_P5_TX[2:0]	R/W	3'h0	31.2[14:12]
3	--	Reserved		0	
2:0	BW_CONTROL_P5_RX[2:0]	BW_CONTROL_P5_RX[2:0]	R/W	3'h0	31.2[10:8]

1.97. Register 0x60(96): reserved address (Value=8'h0D)

Bit	Signal name	Description	R/W	Default	MII_reg
7:4	--	Reserved		4'h0	

3:0	RESERVED_ADD_FORWARD[3:0]	RESERVED_ADD_FORWARD[3:0] Bit3: Reserved MAC address (0180C2000010-0180C20000FF) 1: forward (default), 0: discard. Bit2: Reserved MAC address (0180C2000002- 0180C200000F) 1: forward (default), 0: discard. The default value is the inverted value of pin 69 FILTER_RSV_DA. Bit1:Reserved MAC address (0180C2000001) 1: forward, 0: discard (default) bit0: Reserved MAC address (0180C2000000) 1: forward (default), 0: discard	R/W	4'b1101	30.13[3:0]

1.98. Register 0x61(97): external PHY address (MII0) (Value=8'h00)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4:0	MII0_mac_phy_addr	MII0_mac_phy_addr	R/W	5'h0	31.3[4:0]

1.99. Register 0x62(98): external PHY ability (MII0) (Value=8'h1F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4:0	Capability of external PHY on MII0	Capability of external PHY on MII0 bit12: flow control ability, bit11: 100M full duplex, bit10 : 100M half duplex, bit9 : 10M full duplex, bit8: 10M half duplex	R/W	5'h1f	31.3[12:8]

1.100. Register 0x63(99): external PHY address (MII1) (Value=8'h01)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4:0	MII1_mac_phy_addr	MII1_mac_phy_addr	R/W	5'h01	31.4[4:0]

1.101. Register 0x64(100): external PHY ability (MII1) (Value=8'h1F)

Bit	Signal name	Description	R/W	Default	MII_reg
7:5	--	Reserved		3'h0	
4:0	Capability of external PHY on MII1	Capability of external PHY on MII1 bit12: flow control ability, bit11: 100M full duplex, bit10 : 100M half duplex, bit9 : 10M full duplex, bit8: 10M half duplex	R/W	5'h1f	31.4[12:8]

2. IP175C EEPROM MAPPING TABLE

2.1. Switch ONLY

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Register 00~0F	aa	55	03	0f	98	01	16	10	00	03	00	00	00	9f	9f	9f
Register 10~1F	9f	9f	9f	00	00	00	00	00	01	00	01	00	01	00	01	00
Register 20~2F	02	00	00	00	01	02	00	3f	2f	30	3f	3f	3f	3f	3f	3f
Register 30~3F	3f	3f	3f	3f	3f	3f	3f	01	10	00	00	00	82	00	00	00
Register 40~4F	00	1f	1f	00	00	00	c2	80	01	00	00	00	00	00	00	a0
Register 50~5F	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Register 60~64	0d	00	1f	01	1f											

2.2. One MII (MII0 PHY mode)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Register 00~0F	aa	55	03	0f	98	01	16	11	00	03	00	00	00	9f	9f	9f
Register 10~1F	9f	9f	9f	00	00	00	00	00	01	00	01	00	01	00	01	00
Register 20~2F	02	00	00	00	01	02	00	3f	2f	30	3f	3f	3f	3f	3f	3f
Register 30~3F	3f	3f	3f	3f	3f	3f	3f	01	10	00	00	00	82	00	00	00
Register 40~4F	00	1f	1f	00	00	00	c2	80	01	00	00	00	00	00	00	a0
Register 50~5F	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Register 60~64	0d	00	1f	01	1f											

2.3. Two MII (MII0, MII1 PHY mode)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Register 00~0F	aa	55	03	0f	98	01	16	11	00	03	00	00	00	9f	9f	9f
Register 10~1F	9f	9f	9f	00	00	00	00	00	01	00	01	00	01	00	01	00
Register 20~2F	02	00	00	00	01	02	00	3f	2f	30	3f	3f	3f	3f	3f	3f
Register 30~3F	3f	3f	3f	3f	3f	3f	3f	01	10	00	00	00	82	00	00	00
Register 40~4F	00	1f	1f	00	00	00	c2	80	01	00	00	00	00	00	00	a0
Register 50~5F	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Register 60~64	0d	00	1f	01	1f											

2.4. THREE MII (MII0, MII1 PHY mode, MII2 MAC mode)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Register 00~0F	aa	55	14	0f	98	01	16	11	00	03	00	00	00	9f	9f	9f
Register 10~1F	9f	9f	9f	00	00	00	00	00	01	00	01	00	01	00	01	00
Register 20~2F	02	00	00	00	01	02	00	3f	2f	30	3f	3f	3f	3f	3f	3f
Register 30~3F	3f	3f	3f	3f	3f	3f	3f	01	10	00	00	00	82	00	00	00
Register 40~4F	00	1f	1f	00	00	00	c2	80	01	00	00	00	00	00	00	a0
Register 50~5F	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
Register 60~64	0d	00	1f	01	1f											